an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns in a form such that an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

a dummy pattern supported by the insulating tape adjacent a corner of a region for the semiconductor element to be mounted so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

2. (Amended) The tape for chip on film as defined in claim 1, wherein the dummy pattern is provided independent of the wiring patterns and the solder resist so that the dummy pattern is not in electrical communication with the wiring patterns or the solder resist.

9. (Amended) A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape;

a plurality of wiring patterns formed on the insulating tape; and

a solder resist partially covering the wiring patterns, wherein an opening is defined in the solder resist in an area under the semiconductor element, wherein

a first edge of said opening in the solder resist adjacent a corner of the semiconductor element is located nearer to the corner than a second edge of said opening in the solder resist adjacent the corner different than the first edge so as to control flow of resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

10. (Amended) A tape for chip on film on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns, wherein an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

an inner lead in a wiring pattern located on a specified side of the semiconductor element is at least partially located inside the opening defined in the solder resist, wherein

the inner lead has a large width section wider than an electric connection section of the inner lead connected to the semiconductor element so as to control flow of resin from the specified side to a space between a surface of the semiconductor element and

the insulating tape during resin sealing, so that air bubbles in the resin located in a gap between a surface of the semiconductor element and the insulating tape can be reduced.

11. (Amended) The tape for chip on film as defined in claim 10, wherein the large width section of the inner lead is disposed either outside or inside a border line of a region for the semiconductor element to be mounted, or from outside to inside the border line of the region.

Please add the following new claims:

19. (New) The tape for chip on film of claim 1, wherein the entire dummy pattern is located laterally beyond the periphery of the semiconductor element.

20. (New) The tape for chip on film of claim 1, wherein the dummy pattern is not part of, and is not connected to, the semiconductor element.

21. (New) A tape, for chip on film, on which a semiconductor element is mounted and resin is applied for sealing the semiconductor element, the tape for chip on film comprising:

an insulating tape, wherein the semiconductor element is supported by the insulating tape and no aperture is defined in the insulating tape in an area under the semiconductor element;

a plurality of wiring patterns formed on the insulating tape;

a solder resist partially covering the wiring patterns in a form such that an opening is defined in the solder resist at least in all or part of an area under the semiconductor element; and

a dummy pattern supported by the insulating tape adjacent a corner of the semiconductor element so as to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing, and wherein at least part of the dummy pattern is located laterally beyond a periphery of the semiconductor element so that at least part of an upper surface of the dummy pattern is covered with the resin.

22. (New) The tape for chip on film of claim 6, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape without use of an adhesive.

23. (New) The tape for chip on film of claim 6, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape with use of an adhesive.

24. (New) The tape for chip on film of claim 8, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape without use of an adhesive.

25. (New) The tape for chip on film of claim 8, wherein the wiring pattern, the inner lead, and the dummy pattern are fixed to the insulating tape with use of an adhesive.

26. (New) A semiconductor device comprising a semiconductor element mounted on the tape for chip on film as defined in claim 9 and sealed with resin.

27. (New) A semiconductor device comprising a semiconductor element mounted on the tape for chip on film as defined in claim 10 and sealed with resin.

28. (New) The tape for chip on film of claim 10, wherein the entire dummy pattern is located laterally beyond the periphery of the semiconductor element.

29. (New) The tape for chip on film of claim 11, wherein the entire dummy pattern is located under the semiconductor element without contacting the semiconductor element.

REMARKS

This is in response to the Office Action dated October 23, 2002. New claims 19-29 have been added. Thus, claims 1-29 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"